PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MIC/14/8294
Dated 07 Feb 2014

VFQFPN/ UFQFPN New sources due to Stats ChipPAC Malaysia closure

Table 1. Change Implementation Schedule

Forecasted implementation date for change	11-Jul-2014
Forecasted availability date of samples for customer	11-Jun-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	11-Jun-2014
Estimated date of changed product first shipment	11-Jul-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	VFQFPN / UFQFPN products in Stats ChipPAC Malaysia
Type of change	Package assembly location change
Reason for change	Stats ChipPAC Malaysia line closure
Description of the change	Transfer of VFQFPN / UFQFPN products from Stats ChipPAC Malaysia to Stats ChipPAC China + Additional source for some UFQFPN products at Amkor ATP3 Philippines.
Change Product Identification	see indicated below
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

- -

Customer Acknowledgement of Receipt	PCN MMS-MIC/14/8294
Please sign and return to STMicroelectronics Sales Office	Dated 07 Feb 2014

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Colonna, Daniel	Marketing Manager
Buffa, Michel	Product Manager
Narche, Pascal	Q.A. Manager

PRODUCT/PROCESS CHANGE NOTIFICATION

VFQFPN/ UFQFPN New sources due to Stats ChipPAC Malaysia closure

MMS - Microcontrollers Division (MCD)

Dear Customer,

Stats ChipPAC Malaysia site will close in December 2014.
In order to anticipate this closure and insure expected level of service to our customers, ST MCD Division has decided to transfer the manufacturing of devices housed in VFQFPN / UFQFPN packages from Stats ChipPAC Malaysia to Stats ChipPAC China.
Also, in order to sustain the strong demand, ST MCD Division decided to add an additional source: Amkor Philippines ATP3.

What are the changes?

Change 1 : Transfer of VFQFPN / UFQFPN packages from Stats ChipPAC Malaysia to Stats ChipPAC China.

	Package products	Actual	New
Location	All	Stats ChipPAC Malaysia	Stats ChipPAC China
BOM	UFQFPN 4x4	Same BOM	
	UFQFPN 5x5 & 7x7	Change limited to : - lead frame design (*)	
	VFQFPN 6x6	Changes limited to : - lead frame design (*) - Wire diameter from 1.0 mil to 0.8 mil	

(*) To improve package robustness, it has been decided to generalize the insertion of grooves on lead frame die pad for VFQFPN / UFQFPN packages to better anchor the molding compound into the frame.

Change 2: Additional source for some UFQFPN products at Amkor ATP3 Philippines.

	Package products	Actual	New
Location	All	Stats ChipPAC Malaysia	Amkor ATP3 Philippines
BOM	UFQFPN 4x4	Changes limited to : - Die attach : from Ablestick 8006NS to NSCC NEX-130C - Resin : from Sumitomo G770HCD to Sumitomo G700Y	
	UFQFPN 5x5 UFQFPN 7x7, except STM32Wxx	Changes limited to : - Die attach : from Ablebond 8290 to Dexter 1234-100 - Resin : from Sumitomo G770 to Sumitomo G700Y - lead frame design (*)	

(*) To improve package robustness, it has been decided to generalize the insertion of grooves on lead frame die pad for VFQFPN / UFQFPN packages to better anchor the molding compound into the frame.

Why?

VFQFPN / UFQFPN packages will be permanently transferred to new locations, in order to guaranty the product continuation.

When?

The production on the new locations will start from below dates:

	Package products	Samples availability / Qual results date	Implementation / First shipment date
Transfer to Stats ChipPAC China	UFQFPN 4x4	Week 29	Week 33
	UFQFPN 5x5	Week 24	Week 28
	UFQFPN 7x7, except STM32Wxx	Week 24	Week 28
	UFQFPN 7x7, STM32Wxx	Week 32	Week 36
	VFQFPN 6x6	Week 32	Week 36
	VFQFPN 6x6 STM32Wxx	Week 38	Week 42
Additional source at Amkor ATP3 Philippines	UFQFPN 4x4	Week 41	Week 45
	UFQFPN 5x5	Week 38	Week 42
	UFQFPN 7x7, except STM32Wxx	Week 38	Week 42

How will the changes be qualified?

Changes will be qualified using the standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard. You can find below Qualification Plans on change 1 and change 2.

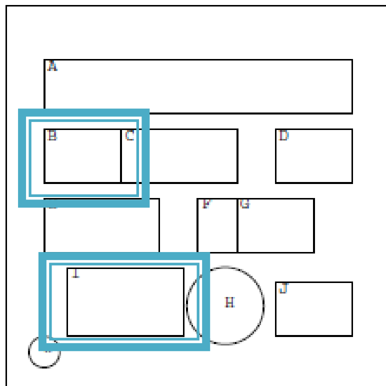
What are the impacts of the changes?

- **Form:** no change
- **Fit:** no change
- **Function:** no change

How can the change be seen?

Traceability of the change is ensured by ST internal tools.

The marking composition indicated on the products is changing from:



B : Assembly plant changes from 9H to :

- Change 1: GH
- Change 2 : 7B

I : Country Of Origin changes from MYS to :

- Change 1 : CHN
- Change 2 : PHL

We remain available to discuss any concern that you may have regarding this Product Change Notification.

With our sincere regards.
Michel Buffa
Microcontroller Division General Manager

List of Commercial Products :

Package products	Commercial products
UFQFPN 4x4	STM32F031G4U6 STM32F031G6U6 STM32F038G4U6 STM32F038G6U6 STM32F042G4U6 STM32F042G6U6 STM32F050G4U6 STM32F050G6U6 STM32F050G6U7 STM32F060G4U6 STM32F060G6U6 STM8L101G2U6 STM8L101G2U6A STM8L101G2U6TR STM8L101G3U6 STM8L101G3U6A STM8L101G3U6TR STM8L151G2U6 STM8L151G3U3 STM8L151G3U6 STM8L151G3U6TR STM8L151G4U3 STM8L151G4U6 STM8L151G4U6TR STM8L151G6U3 STM8L151G6U3TR STM8L151G6U6 STM8L151G6U6TR STM8L151G6U7 STM8L151G6U7TR STM8LP101G2MBJTR STM8LP101G2MCXTR STM8T243GU6MEBTR STM8T243GU6MEDTR STM8TL52G4U6 STM8TL52GU6IQRTR STM8TL52GU6MCUTR STM8TL52GU6MEUTR STM8TL53G4U6 STM8TL53GU6MFFTR
UFQFPN 5x5	2AP00100TCUSTOM 2AP00179TCUSTOM STM32F031K4U6 STM32F031K6U6 STM32F038K4U6 STM32F038K6U6 STM32F042K4U6 STM32F042K6U6 STM32F050K4U6 STM32F050K6U6 STM32F050K6U7

	STM32F051K4U6 STM32F051K4U6TR STM32F051K4U7 STM32F051K4U7TR STM32F051K6U6 STM32F051K6U6TR STM32F051K6U7 STM32F051K6U7STR STM32F051K6U7TR STM32F051K8CRQTR STM32F051K8U6 STM32F051K8U6TR STM32F051K8U7 STM32F051K8U7TR STM32F060K4U6 STM32F060K6U6 STM32F061K8U6 STM32F301K8U6 STM32F302K8U6 STM32F311K8U6 STM32P051K8MBOTR STM8L101K3U6 STM8L101K3U6TR STM8L151K2U6 STM8L151K3U3 STM8L151K3U6 STM8L151K4U6 STM8L151K4U6TR STM8L151K6U3 STM8L151K6U6 STM8L151K6U6TR STM8L152K4U6 STM8L152K6U6 STM8L152K6U6TR STM8LP151K4LIOTR STM8LP151K4LIZTR STM8LP151K4U6XXM STM8S103K3U6 STM8S103K3U6TR STM8S105K4U6A STM8S105K6U6A STM8S105K6U6ATR STM8S903K3U3 STM8S903K3U3TR STM8S903K3U6 STM8S903K3U6TR STM8SP103K3MBETR STM8SP103K3MCSTR STM8SP103K3U6MCS STM8SP903K3MBLTR STM8SP903K3MCITR
UFQFPN 7x7, except STM32Wxx	STM32F042C6U6 STM32F048C6U6 STM32F051C6U6 STM32F051C8U6 STM32F052CBU6 STM32F071CBU6

	STM32F072C8U6 STM32F072CBU6 STM32F101C8U6 STM32F101C8U6TR STM32F101CBU6 STM32F103C6U6A STM32F103CBU6 STM32F401CBU6 STM32F401CCU6 STM32F401CCU6U STM32F401CDU6 STM32F401CEU6 STM32L100C6U6 STM32L151C6U6 STM32L151C6U6TR STM32L151C8U6 STM32L151C8U6TR STM32L151CBU6 STM32L151CBU6A STM32L151CBU6TR STM32L151CCU6 STM32L152C6U6 STM32L152C8U6 STM32L152CBU6 STM32L152CBU6A STM32L152CCU6 STM32L152CCU6D STM32P101C8MBHTR STM32P101C8MBKTR STM8L151C4U6 STM8L151C4U6TR STM8L151C6U3 STM8L151C6U6 STM8L151C8U3 STM8L151C8U6 STM8L151C8U6TR STM8L152C4U6 STM8L152C6U3 STM8L152C6U6 STM8L152C8U6 STM8TL53C4U6 STM8TL53C4U6A STM8TLP53C4MBSTR STM8TLP53C4MEOTR
UFQFPN 7x7, STM32Wxx	STM32W108C8U63TR STM32W108C8U64TR STM32W108CBU6 STM32W108CBU63TR STM32W108CBU64TR STM32W108CBU66TR STM32W108CCU73TR STM32W108CCU74TR STM32W108CCU75TR STM32W108CCU7TR STM32W108CZU73TR STM32W108CZU74TR STM32W108CZU75TR

VFQFPN 6x6, except STM32Wxx	STM32F101T8U6 STM32F101T8U6TR STM32F101TBU6 STM32F102T8U6TR STM32F103T8U6 STM32F103T8U6BCD STM32F103T8U6TR STM32F103T8U7 STM32F103T8U7TR STM32F103TBU6 STM32F103TBU7 STM32P103T8ABC STM32F101T4U6A STM32F101T6U6A STM32F101T6U6ATR STM32F103T4U6A STM32F103T6U6A STM32F103T6U7A
VFQFPN 6x6, STM32Wxx	STM32W108HBU63 STM32W108HBU63TR STM32W108HBU6 STM32W108HBU64TR

RERMCD 1315 RELIABILITY PLAN

Qualification of :

<u>VFQFPN and UQFPN at Stats ChipPac China for Microcontrollers devices</u>

Qualification Reference:	**RERMCD1315**
Issued on:	**Jan 17, 2014**
Assembly Plant:	**Stats ChipPac China (SCC)**
Assembly Line:	**VFQFPN- UFQFPN**
Devices:	**MCD Standard products**
Package / Process:	**5x5 (32 Leads) 7x7 (48 Leads)** **4x4 COL (28 Leads)** **6x6 (36 Leads- 40 Leads)**
MSL:	**MSL3**

Purpose

Qualification of new assembly lines for VFQFPN and UFQFPN packages assembled at SCC (China).

Test Vehicles :

Package line	Assembly Line	Package	Device (Partial RawLine Code)	Diffusion Process	Number of Lots
1	UFQFPN 5x5_7x7	5x5-32L Pure Sn	STM32F (MI*440) STM8S (MI*767) STM32L (MI*416)	TSMC F9GO1 F9GO2	**1** **1** *1 Monitoring*
		7x7- 48L Pure Sn	STM32F (MG*410) STM32F (MG*423)	TSMC M10	**1** *1 Monitoring*
		7x7- 48L PPF	STM32W (MG*N351)	TSMC	*1 Monitoring*
2	UFQFPN 4x4 COL	4x4- 28L PPF	STM32F (MB*444) STM8L (MB*761) STM8T (MB*769)	TSMC F9GO2 F9GO2	**1** **1** **1**
3	VFQFN 6x6	6x6- 36L Pure Sn	STM32F (ZR*410) STM32F (ZR*412)	TSMC	**2** **1**
		6x6- 40L Pure Sn	STM32W (ZF*N350)	TSMC	*1 Monitoring*

Package Reliability Trials :

(*) tests performed after preconditioning

Reliability Trial		**Test Conditions**	**Pass Crite-ria**	**Unit per Lot**	**Qual Lot nb**
PC	Pre Conditioning: Moisture Sensitivity Jedec Level 3 J-STD-020/ JESD22-A113	Bake (125°C / 24 hrs) Soak (30°C / 60% RH / 192 hrs) for level 3 Convection reflow: 3 passes with Jedec level 3	3 passes MSL3	**308**	**3/ package lines**
AC or Uhast(*)	Autoclave JESD22 A102 UnBiased Highly Accelerated Temperature and Humidity Stress JESD22 A118	121°C, 100% RH, 2 Atm 130°C, 85%RH, 2 atm	96h	**77**	**3/ package lines**
TC(*)	Thermal Cycling JESD22 A104	-50°C, +150°C	1000Cy	**77**	**3/ package lines**
THB(*)	Temperature Humidity Bias JESD22 A101	85°C, 85% RH, bias	1000h	**77**	**3/ package lines**

THS(*)	Temperature Humidity Storage JESD22 A110	85°C, 85% RH, no bias	1000h	**77**	**3/ package lines**
HTSL	High Temperature Storage Life JESD22 A103	150°C- no bias	1000h	**77**	**3/ package lines**
ESD	ESD Charge Device Model JESD22-C101	750V corners 500V all other pins	750V / 500V	**3**	**All devices**
Physical dimension	Dimension measurement JESD 22B100/B108		CPK >1.33 PPK >1.67	**10**	**1 lot /package line**
Solderability	Lead solderability JESD 22B102		>95% lead cover-age	**45 leads**	**1 lot /package line**
WBP	Wire Bond Pull Mil Std 883 Method 2011		Mini-mum pull strength after TC=3 grams after TC	**30 wires**	**3/ VQFN6*6**
WBS	Wire Bond Shear AEC Q100-001		Min bond shear 15g after TC	**30 wires**	**3/ VQFN6*6**

Attachment : Reliability tests description

Package oriented tests/ Trials description

1. Preconditioning

According to ST spec 0098044.
Preconditioning test sequence simulates storage and soldering of SMD (surface mount devices) before submitting them to the reliability tests. It aims to validate the moisture sensitivity level of the package, and prepare it to the stress of additional reliability tests, thus enabling a good modelization of the life of the packaged product.
Out-of-bag floor life storage and soldering are modeled by the following test sequence:

- Bake to completely remove moisture from the package;
- Moisture soak according to the package moisture level;
- IR reflow.

The aim is to check that the chip and plastic package withstand the stress due to report on card. Depending on their technology, packages may absorb moisture during their transportation and/or storage, moisture that is released during the soldering operation. At this step, the moisture absorbed is vaporized due to high temperature of solder report process. This phenomenon can cre-

ate plastic swelling, "pop corn" effect, and cracks which eventually results in wire breakage, passivation cracks, and delamination.

2. **Autoclave (AC)**

The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.
Purpose: to investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
To point out critical water entry paths with consequent electrochemical and galvanic corrosion.

1. **Unbiased Highly Accelerated Temperature and Humidity Stress (UHAST)**

The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solidstate devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is is used to identify failure mechanisms internal to the package and is destructive.

2. **Temperature Cycling (TC)**

The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere (thermal gradient typical 10 C/min).
Purpose: to investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system.
Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die-attach layer degradation.

3. **Temperature Humidity Bias (THB)**

The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.

The Temperature Humidity Bias follows the same method than HAST at lower temperature.

Purpose: to investigate failure mechanisms activated in the die-package environment by electrical field and wet conditions.
Typical failure mechanisms are electro-chemical corrosion and surface effects related to the molding compound.
The package moisture resistance with electrical field applied is verified, both electrolytic and galvanic corrosion are put in evidence.

Conditions:

- Ta=85°C; R.H.=85%;
- Power supply voltage less or equal to max operative voltage to not exceed Tj = 95 °C.

4. Temperature Humidity Storage (THS)

The Temperature Humidity Storage is stored at controlled conditions of high temperature and relative humidity.

The Temperature Humidity Storage follows the same method than Unbiased HAST at lower temperature.

Purpose: to evaluate the reliability of non-hermetic packaged solid-state devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.
Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to identify failure mechanisms internal to the package.

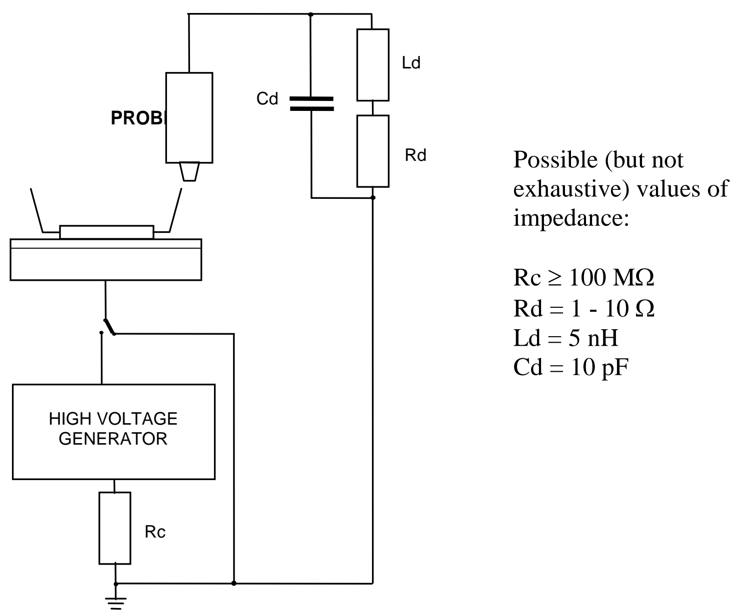
- Test conditions: 85°C / 85% RH.
- No power supply

5. High Temperature Storage Life (HTSL)

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
Purpose: to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.

1. ESD Charge Device Model (CDM)

This ESD failure model is associated with the device and package itself. The CDM is intended to simulate charging/discharging events that occur in production equipment and processes. The Field induced CDM equivalent circuit used to describe this phenomenon is illustrated in Figure 1.



Possible (but not exhaustive) values of impedance:

Rc ≥ 100 MΩ
Rd = 1 - 10 Ω
Ld = 5 nH
Cd = 10 pF

Fig.1 : Field induced CDM equivalent circuit

RERMCD 1321 RELIABILITY PLAN

Qualification of :

UQFPN at AMKOR Philippines
for Microcontrollers devices

Qualification Reference:	**RERMCD1321**
Issued on:	**Jan 17, 2014**
Assembly Plant:	**AMKOR Philippines (ATP)**
Assembly Line:	**VFQFPN- UFQFPN**
Devices:	**MCD Standard products**
Package / Process:	**5x5 (32 Leads) 7x7 (48 Leads)** **4x4 COL (28 Leads)**
MSL:	**MSL3**

Purpose

Qualification of package UFQFPN assembled on production lines at ATP (Philippines).

Test Vehicles :

Assembly line	Package Line	Package	Device (Partial RawLine Code)	Diffusion Process	Number of Lots
1	UFQFPN 5x5_7x7	5x5-32L Pure Sn	STM32F (MI*440) STM8S (MI*767)	TSMC F9GO1	**1** **1**
		7x7- 48L Pure Sn	STM32F (MG*410)	TSMC	**1**
2	UFQFPN 4x4 COL	4x4- 28L PPF	STM8T (MB*769) STM8L (MB*764) STM32F (MB*444)	F9GO2 F9GO2 TSMC	**1 (*)** ***1 as monitoring*** ***1 as monitoring***

(*) 1 qualification lot as qualification by similarity with UFQFPN3*3 COL already qualified for MCD devices: report reference MCDRER1205

Package Reliability Trials :

(*) tests performed after preconditioning

Reliability Trial		Test Conditions	Pass Criteria	Unit per Lot	Qual Lot nb/ package
PC	Pre Conditioning: Moisture Sensitivity Jedec Level 3 J-STD-020/ JESD22-A113	Bake (125°C / 24 hrs) Soak (30°C / 60% RH / 192 hrs) for level 3 Convection reflow: 3 passes with Jedec level 3	3 passes MSL3	**308**	**3/ 5x5-7x7** **1/ 4x4**
AC or Uhast(*)	Autoclave JESD22 A102 UnBiased Highly Accelerated Temperature and Humidity Stress JESD22 A118	121°C, 100% RH, 2 Atm 130°C, 85%RH, 2 atm	96h	**77**	**3/ 5x5-7x7** **1/ 4x4**
TC(*)	Thermal Cycling JESD22 A104	-50°C, +150°C	1000Cy	**77**	**3/ 5x5-7x7** **1/ 4x4**
THB(*)	Temperature Humidity Bias JESD22 A101	85°C, 85% RH, bias (3.6V)	1000h	**77**	**3/ 5x5-7x7** **1/ 4x4**
THS(*)	Temperature Humidity Storage JESD22 A110	85°C, 85% RH, no bias	1000h	**77**	**3/ 5x5-7x7** **1/ 4x4**

HTSL	High Temperature Storage Life JESD22 A103	150°C- no bias	1000h	**77**	**3/ 5x5-7x7** **1/ 4x4**
ESD	ESD Charge Device Model JESD22-C101	750V corners 500V all other pins	750V / 500V	**3**	**All devices**
Physical dimension	Dimension measurement JESD 22B100/B108		CPK >1.33 PPK >1.67	**10**	**1 lot /package line**
Solderability	Lead solderability JESD 22B102		>95% lead cover-age	**45 leads**	**1 lot /package line**

Attachment : Reliability tests description

Package oriented tests/ Trials description

1. Preconditioning

According to ST spec 0098044.
Preconditioning test sequence simulates storage and soldering of SMD (surface mount devices) before submitting them to the reliability tests. It aims to validate the moisture sensitivity level of the package, and prepare it to the stress of additional reliability tests, thus enabling a good modelization of the life of the packaged product.
Out-of-bag floor life storage and soldering are modeled by the following test sequence:

- Bake to completely remove moisture from the package;
- Moisture soak according to the package moisture level;
- IR reflow.

The aim is to check that the chip and plastic package withstand the stress due to report on card. Depending on their technology, packages may absorb moisture during their transportation and/or storage, moisture that is released during the soldering operation. At this step, the moisture absorbed is vaporized due to high temperature of solder report process. This phenomenon can create plastic swelling, "pop corn" effect, and cracks which eventually results in wire breakage, passivation cracks, and delamination.

2. Autoclave (AC)

The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.
Purpose: to investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
To point out critical water entry paths with consequent electrochemical and galvanic corrosion.

1. Unbiased Highly Accelerated Temperature and Humidity Stress (UHAST)

The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solidstate devices in humid environments. It is a highly accelerated test which employs

temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is is used to identify failure mechanisms internal to the package and is destructive.

2. Temperature Cycling (TC)

The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere (thermal gradient typical 10 C/min).
Purpose: to investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system.
Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die-attach layer degradation.

3. Temperature Humidity Bias (THB)

The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.

The Temperature Humidity Bias follows the same method than HAST at lower temperature.

Purpose: to investigate failure mechanisms activated in the die-package environment by electrical field and wet conditions.
Typical failure mechanisms are electro-chemical corrosion and surface effects related to the molding compound.
The package moisture resistance with electrical field applied is verified, both electrolytic and galvanic corrosion are put in evidence.

Conditions:

- Ta=85°C; R.H.=85%;
- Power supply voltage less or equal to max operative voltage to not exceed Tj = 95 °C.

4. Temperature Humidity Storage (THS)

The Temperature Humidity Storage is stored at controlled conditions of high temperature and relative humidity.

The Temperature Humidity Storage follows the same method than Unbiased HAST at lower temperature.

Purpose: to evaluate the reliability of non-hermetic packaged solid-state devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.
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- Test conditions: 85°C / 85% RH.
- No power supply

5. High Temperature Storage Life (HTSL)

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
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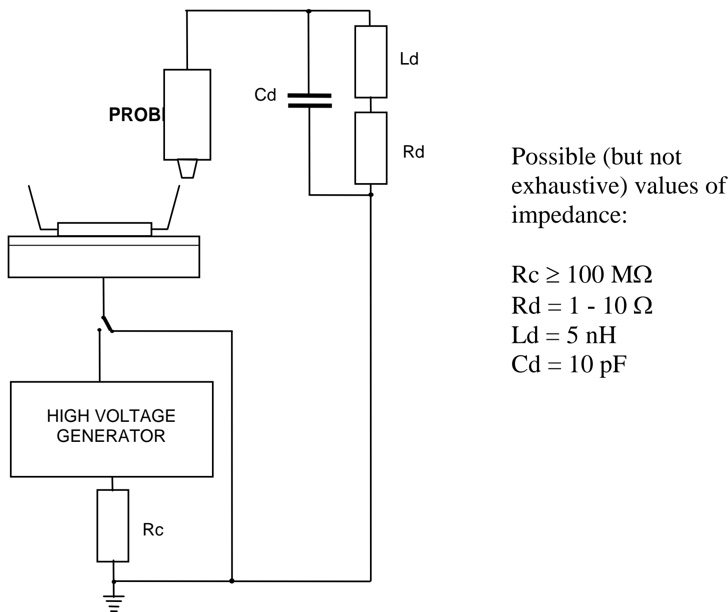

Possible (but not exhaustive) values of impedance:

Rc ≥ 100 MΩ
Rd = 1 - 10 Ω
Ld = 5 nH
Cd = 10 pF

Fig.1 : Field induced CDM equivalent circuit

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